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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. BOX 2938  
MINNEAPOLIS, MN 55402

EXAMINER

GUHARAY, KARABI

ART UNIT

PAPER NUMBER

2879

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/145,595	LEE, JI UNG	
	Examiner Karabi Guharay	Art Unit 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  
 If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  
 If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  
 Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  
 Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on \_\_\_\_\_.  
 2a) This action is **FINAL**.                                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 36-60 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 36-60 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
     If approved, corrected drawings are required in reply to this Office action.  
 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) All    b) Some \* c) None of:  
         1. Certified copies of the priority documents have been received.  
         2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
     a) The translation of the foreign language provisional application has been received.  
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)                                    4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)                    5) Notice of Informal Patent Application (PTO-152)  
 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                    6) Other: \_\_\_\_\_.

***Response to Amendment***

Amendment C, filed on January 17, 2002 has been entered.

Amendment of claim 43 overcomes the objection of claim 43.

Amendments of claims 47, 51, 52, 53, and 57 overcome the rejection of claims 47-60 under 35 U.S.C. 112 second paragraph.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 36-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al. (U.S. 5,653,619).

Regarding claim 36, Cloud et al. disclose a field emission device (see column 1, line 15) comprising a number of cathodes formed in rows along a substrate (11), a gate insulator (18) formed along the substrate and surrounding the cathodes (see Fig 1), a number of gate lines (15) formed on the gate insulator (18) (see column 1, lines 60-67), an anode (16) (column 4, lines 6-7) being formed orthogonal and opposing the cathodes (column 2, lines 13-14).

Cloud et al. do not exemplify the anode in form of strips (plurality of anodes). However, It is conventional to have number of anodes in matrix-addressed array of cold cathode emission devices (see U.S. 5,675,210).

Cloud et al. further disclose that a distance separating the number of cathode emitter tips from the number of gate lines is significantly thinner than a separation distance separating the number of gate lines and the substrate (see Fig 1, Fig 2, and Fig 2B).

Method limitations in claim 36 and claim 37 have not been given patentable weight since the method of forming the device is not germane to the issue of patentability of the device itself (see MPEP 2113).

Regarding claim 38, Cloud et al. disclose that the number of cathodes (13) include polysilicon cones (see column 3, lines 60-66).

Regarding claim 39, Cloud et al. disclose that the cathodes (13) include metal silicides on the polysilicon cones (see column 7, lines 54-59).

Regarding claim 40, Cloud et al. disclose that the substrate (11) includes glass (column 3, line 58).

Regarding claim 41, Cloud et al. disclose that gate lines (15) include refractory metals (column 6, lines 1-2).

Regarding claim 42, Cloud et al. disclose that the number of gate lines (15) include doped silicon (column 6, lines 2-3).

Claim 43 recites essentially all the limitations of claim 36 (see rejection of claim 36) together with a row decoder and column decoder to selectively access the pixels and a processor. Though Cloud does not exemplify these elements but these are intrinsic to any flat panel display system for displaying images.

Claim 44 is rejected for the same reason as claim 37.

Claim 45 is rejected for the same reason as claim 39.

Claim 46 is rejected for the same reason as claim 41.

Regarding claim 47, Cloud et al. disclose a field emission device (see column 1, line 15) comprising a number of cathodes formed in rows along a substrate (11), a gate insulator (18) formed along the substrate and surrounding the cathodes (see Fig 1), the gate insulator having a gate line region thickness (thickness of the insulator 18, in Fig 1, Fig 2 and Fig 2B) a number of gate lines (15) coupled to the gate insulator (18) (see column 1, lines 60-67), the distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness (see Fig 2a, and Fig 2B), an anode (16) (see column 4, lines 6-7) being formed orthogonal and opposing the cathodes (see column 2, lines 13-14).

Cloud et al. do not exemplify the anode in form of strips (plurality of anodes). However, It is conventional to have number of anodes in matrix-addressed array of cold cathode emission devices (see U.S. 5,675,210).

Claim 48 recites essentially the same limitation of claim 38. Thus claim 48 is rejected as claim 38 (see rejection of claim 38).

Claim 49 recites essentially the same limitation of claim 41. Thus claim 49 is rejected as claim 41 (see rejection of claim 41).

Claim 50 recites essentially the same limitations of claim 42. Thus claim 50 is rejected as claim 42 (see rejection of claim 42).

Regarding claim 51, Cloud et al. disclose a field emission device (see column 1, line 15) comprising a number of cathodes formed in rows along a substrate (11), a gate

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insulator (18) formed along the substrate and surrounding the cathodes (see Fig 1), the gate insulator having a gate line region thickness (thickness of the insulator 18, in Fig 1, Fig 2 and Fig 2B) a number of gate lines (15) coupled to the gate insulator (18) (see column 1, lines 60-67), the distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness (see Fig 2a, and Fig 2B), an anode (16) (see column 4, lines 6-7) being formed orthogonal and opposing the cathodes (see column 2, lines 13-14), wherein the number of cathodes include metal silicides on the polysilicon cones (see column 7, lines 54-59).

Cloud et al. do not exemplify the anode in form of strips (plurality of anodes). However, It is conventional to have number of anodes in matrix-addressed array of cold cathode emission devices (see U.S. 5,675,210).

Regarding claim 52, Cloud et al. disclose a field emission device (see column 1, line 15) comprising a number of cathodes formed in rows along a substrate (11), a gate insulator (18) formed along the substrate and surrounding the cathodes (see Fig 1), the gate insulator having a gate line region thickness (thickness of the insulator 18, in Fig 1, Fig 2 and Fig 2B) a number of gate lines (15) coupled to the gate insulator (18) (see column 1, lines 60-67), the distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness (see Fig 2a, and Fig 2B), an anode (16) (see column 4, lines 6-7) being formed orthogonal and opposing the cathodes (see column 2, lines 13-14).

Cloud et al. do not exemplify the anode in form of strips (plurality of anodes).

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However, It is conventional to have number of anodes in matrix-addressed array of cold cathode emission devices (see U.S. 5,675,210).

Cloud et al. also do not exemplify that the substrate is a semiconductor on glass substrate, but teach that any variety of suitable substrate can be used (line 59 of column 2). However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use semiconductor on glass substrate, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claim 53 Cloud et al. discloses a flat panel display (line 42 of column 2) comprising a field emitter array (column 1, line 15) including essentially all the limitations of claim 47 (see rejection of claim 47) together with limitations of a row decoder and a column decoder to selectively access the pixels and a processor. Though Cloud does not exemplify these elements but these are intrinsic to any flat panel display system for displaying images.

Claim 54 recites essentially the same limitation of claim 37. Thus claim 54 is rejected as claim 37 (see rejection of claim 37).

Claim 55 recites essentially the same limitations of claim 39. Thus claim 55 is rejected as claim 39 (see rejection of claim 39).

Claim 56 recites essentially the same limitations of claim 41. Thus claim 56 is rejected as claim 41 (see rejection of claim 41).

Regarding claim 57 Cloud et al. disclose a flat panel display (line 42 of column 2) comprising a field emitter array (see column 1, line 15) comprising a number of

cathodes formed in rows along a substrate (11), a gate insulator (18) formed along the substrate and surrounding the cathodes (see Fig 1), the gate insulator having a gate line region thickness (thickness of the insulator 18, in Fig 1, Fig 2 and Fig 2B) a number of gate lines (15) coupled to the gate insulator (18) (see column 1, lines 60-67), the distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness (see Fig 2a, and Fig 2B), an anode (16) including phosphor (see column 4, lines 6-7) being formed orthogonal and opposing the cathodes (see column 2, lines 13-14).

Cloud et al. do not exemplify the anode in form of strips (plurality of anodes), including multiple phosphors. However, it is conventional to have number of anodes in matrix-addressed array of cold cathode emission devices (see U.S. 5,675,210).

Claim 58 recites essentially the same limitation of claim 37. Thus claim 58 is rejected as claim 37 (see rejection of claim 37).

Claim 59 is rejected as claim 39.

Claim 60 is rejected as claim 41.

### ***Response to Arguments***

Applicant's arguments have been fully considered but they are not persuasive.

(1) Regarding applicant's argument of "method limitations carry patentable weight in a product-by-process claim", examiner wants to emphasize that even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself (see MPEP 2113). A comparison of the recited process with the prior art processes does not resolve the issue concerning

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patentability of the product. See *In Re Fessman*, 489 F2d 742, 180 USPQ 324 (CCPA 1974).

If the product in the product-by-process claim is same as or obvious from a product of the prior art, claim is unpatentable even though the prior product was made by a different process. *In Re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed Cir. 1985).

(2) Applicant argued that the structure defined as "a distance separating the number of cathode emitter tips from the number of gate lines is significantly thinner than a separation of the number of gate lines and the substrate" is novel over the Cloud reference, and cannot be inferred from the figures, since the figures cited in the rejection (Fig 1, 2, 2A, 2B) are not drawn to the scale.

In response to above argument, examiner agrees that Cloud does not disclose that the figures are drawn to scale. However, applicant mentioned, "drawings must be interpreted in light of specification". In this respect, examiner points out that Fig 2A, and Fig 2B, have been interpreted in light of specification, as evidenced in column 5, lines 52-57. Here Cloud teaches that the insulating layer 18 can be deposited to a level substantially equal to or slightly higher than the level of the cathode tips (lines 52-55 of column 5). In case when it is deposited at the level of cathode tip, thickness of the insulating layer 18 above the cathode tip is zero while the thickness of the insulating layer at other locations has a definite value. In case it is deposited slightly higher than the tip of the cathode, thickness of the insulating layer is much less at the tip of the cathode compared to thickness of the insulating layer in other locations (mainly at the

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locations where emissive cones are not located). Since thickness of the insulating layer is smaller above the cathode tip compared to other region in Fig 2A, and Fig 2B, (see lines 52-55 of column 5) the gate layer 15 is closer to the cathode, in other words, distance separating cathode emitter tip to the gate lines are thinner than the distance separating gate lines and the substrate.

(1) Applicant argues that cloud does not teach variations in thickness. However, examiner wants to point out that Cloud teaches that the insulating layer 18 can be deposited to a level substantially equal to or slightly higher than the level of the cathode tips (lines 52-55 of column 5). In the case, when it is deposited at the level of cathode tip, thickness of the insulating layer 18 above the cathode tip is zero while the thickness of the insulating layer at other locations has a definite value. In case it is deposited slightly higher than the tip of the cathode, thickness of the insulating layer is much less at the tip of the cathode compared to thickness of the insulating layer in other locations (mainly at the locations where emissive cones are not located). Thus Cloud does teach variations in the thickness of the insulating layer 18. Consequently Cloud creates non-uniform thickness of the insulating layer 18, as applicant's non-uniform insulating layer.

Applicant emphasized that Cloud teaches conformal insulating layer, here it should be noted that Cloud teaches that the insulating layer 18 of Fig 3, is preferably a conformal insulating layer (see lines 61-62 of column 5). Thus, in case of Fig 3, thickness of the insulating layer is uniform, not in case of Fig 2A, and Fig 2B.

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***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is (703) 305-1971. The examiner can normally be reached on Monday-Friday 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (703) 305-4794. The fax phone numbers for the organization is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K. G.  
Karabi Guharay  
Patent Examiner  
Art Unit 2879

  
NIMESHKUMAR D. PATEL  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800